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Resume

Education

2022–2027 **Ph.D in EECS**, *University of Michigan*, *Ann Arbor* .

2016–2021 **B.Tech Dual in ECE**, *IIIT*, *Hyderabad* .

Working Experience

Jan 2023 to present **Graduate Student Research Assistant in MICL Lab, UMich, Ann Arbor**.
Working on programmable matter project, under the guidance of Dr. David Blaauw.

Jun 2021 to July 2022 **Analog enginner at Texas Instruments** .

1. I worked on the design of package stress-resilient oscillators and precision op-amps for low power IoT applications. Familiar with verilog A modelling, and worked with such models to characterize stress and also for calibration purposes.

Jan 2021 to Aug 2021 **Research Collaboration with Prof. Inhee Lee**.

1. Designed a 1KHz oscillator with 6.75nW power consumption, for a wide temperature range of -40^0C to 170^0C, operable from 0.65V supply for high temperature applications like oil well monitoring etc. Without any trimming, Typical and Worst case Accuracies are $17ppm/^0C$ and $177ppm/^0C$ respectively, While typical and worst case line sensitivity are $0.3\%/V$ and $2.3\%/V$ respectively.
2. Also Designed an alternative novel architecture that reduces the power consumption of timer without using physically large resistances.
3. Designed a 0.4pJ/cycle (state-of-the-art FoM) Resistance to digital converters to sense the soil fertility.

May to Dec 2020 **SOC Design Intern at Intel Bangalore**.

1. Designed a current reference (from scratch) with 3x programmability in absolute value and 1.5x programmability in temperature coefficient for biasing FLL.
2. Proposed a novel current reference with programmable temperature coefficient considering the system level constraints and new device characteristics in lower technology nodes.
3. Have done aging verification for Intel Ips. This includes finding Bias Temperature Instability (BTI), Hot Carrier Injection (HCI) and mobility degradation components and verifying whether they are in reliability limits. I have also verified the same Ip for Electrical Overstress (EOS) and Electrostatic discharge (ESD).
4. Have done Electromigration and IR analysis (EMIR) using Intel totem tool for RF Ips.

Jan 2020 to April 2020 **Research Collaboration with Khanh Le** .
Designed process monitors, Low dropout regulators and other relevant circuits for the project 'self-adaptive circuit design'. The abstract idea is to correct the increasing PVT and mismatch variations in lower tech nodes using ML models.

May to July 2019 **Research Intern at IIT Madras with Dr Shanthi Pavan** .
Designed fifth order programmable active chebyshev filters for 200X wide tunable range, pass band ripple of 0.5dB, dynamic range of 60dB and non-linearity of -80dB.

May,2018 to Jan 2019 **Low Power Analog Design Intern at BLUESEMI R&D**.
Designed 120nW Temperature to a Digital Converter for wide temperature range of -55^{o}C to 125^{o}C with $< 1^0C$ worst-case inaccuracy after single-point calibration. This sensor was taped out and powered with RF energy harvesting, and the product has got national recognition.

June,2017 to June 2021 **Researcher at CVEST,IIITH (Low Power Analog Designing for IoT Applications)** .
Designed voltage/current references, op-amps, voltage to time converters, flash ADC, SAR ADC, sub-ranging ADC, Schmitt trigger, Gilbert cell, time to voltage converter, always-on comparator with hysteresis, latched comparators with low kick back noise, oscillators and temperature sensors for ultra-low power/low voltage applications under the guidance of Dr. Zia Abbas.

Publications

MS Thesis **Ultra-Low Power Integrated Circuits for Low Power IoT Systems** .
Ashfakh Ali

US PATENT **Proportional to absolute temperature (ptat) voltage generating circuit for generating a ptat voltage and acts as a temperature sensor**.
Abhishek, Ashfakh, Arpan Jain and Zia Abbas.

ISCAS 2023 USA **A 6.75nW, 1kHz, -40-170C Relaxation Oscillator Using Switch Leakage Cancellation Scheme for Low Power High-Temperature IoT Systems**.
Ashfakh Ali, Abhishek Pullela, Ehab Hameed, Arpan Jain, Naveen, Inhee Lee and Zia Abbas

ISCAS 2023 USA **A 0.5V,pico-watt, 0.06%/V 0.03%/V low supply sensitive current/voltage reference without using resisotors and amplifiers**.
Sahishnavi, Sampath, Ashfakh Ali, Inhee Lee and Zia Abbas

ISCAS 2023 USA **A 162nW, 0.845pJ/step Resistance-to-Digital Converter for Miniature Battery-Powered Sensing Systems**.
Arnab, Ashfakh Ali, Arpan Jain, Abhishek, Inhee Lee and Zia Abbas

ISCAS 2023 USA **A 2.3nW Gate-Leakage Based Sub-Bandgap Voltage Reference with LS of 0.0066%/V from -40 to 150C for Low Power IoT Systems**.
Arnab, Barathwaj, Ashfakh Ali, Abhishek and Zia Abbas

ISCAS 2022 USA **A 156pW Gate-Leakage based Voltage/Current Reference for Low Power IoT Systems**.
Abhishek Pullea, Ashfakh Ali, Arpan Jain, Inhee Lee and Zia Abbas

VLSID 2022 India **A 180-degree Phase Shift Biasing Technique for Realizing High PSRR in Low Power Temperature Sensors**.
Arpan Jain, Abhishek Pullela, Ashfakh Ali and Zia Abbas

ISCAS 2021 Korea **A 419pW Process Invariant Temperature Sensor for Ultra-Low Power Microsystems** .
Abhishek Pullela, Ashfakh Ali, Arpan Jain and Zia Abbas

MWSCAS 2021 USA **A 443pW Accumulation-Mode Gate- Leakage Based Bandgap Reference for IoT Applications**.
Abhishek Pullela, Ashfakh Ali, Sushanth Reddy, Arpan Jain and Zia Abbas

MWSCAS 2020 USA **A Sub-nW Current Reference Consuming Constant Power w.r.t Temperature and Process**, *3 Citations*.
Ashfakh Ali, Abhishek Pullela, Arpan Jain and Zia Abbas.

INDIAN PATENT **An On-Chip CMOS Resistance Amplifier**.
Arpan Jain, Ashfakh Ali and Zia Abbas.

INDIAN PATENT **Constant Reference Voltage/Current Generating Circuit**.
Abhishek, Ashfakh, Arpan Jain and Zia Abbas.

VLSI-SOC 2019, Peru **A 47nW, 0.7-3.6V Wide Supply Range, Resistor Based Temperature Sensor for IoT Applications**.
Ashfakh Ali, Arpan Jain, Sai Kiran and Zia Abbas

ISCAS 2019 Japan — **A High PSRR, Stable CMOS Current Reference Using Process Insensitive TC of Resistance for Wide Temperature Applications**.
Arpan Jain, Ashfakh Ali, Sai Kiran and Zia Abbas

Awards

TI Analog 201 Winner — Awarded $200 worth courses from **Dr. Allen Phillip** (Georgia tech professor and Texas Instruments 201 course Instructor) as a prize.

Patent Award 2024 — For two granted patents in Jan and Feb of 2024, that were filed in my undergraduate

Dean's List — Selected in the Dean's list for **Academic Excellence** for 3-semesters from 2017-19.

Research Award — Selected for **IIITH research award** for publishing papers in international conferences during under graduation

Outstanding Thesis Award Nominee — Thesis titled **"Ultra low power Integrated circuits for low power IoT Systems"** is one of the four thesis nominated from the whole University **Outstanding Thesis Award**.

Teaching Experience

Jan 2020 to April 2020 — **Teaching Assistant for Analog Electronic Circuits** .
Role: Took classes on topics like negative feedback op amp circuits, oscillators, RC circuits

Aug 2019 to Dec 2019 — **Teaching Assistant for Analog IC Design** .
Role: Took classes on topics like negative feedback, current mirrors, Low power PVT invariant designs etc and guided projects on current reference and temperature sensors.

January to April 2019 — **Teaching Assistant for Electronic Workshop II** .
Role: Coordinated with faculty in designing assignments, projects and lab exercises.

August to November 2018 — **Teaching Assistant for Linear Electronic Circuits** .
Role: Lectured on topics like Negative Feedback techniques in Biasing, Current Mirrors and Single Stage Amplifiers

Major Digital Design Projects

Aug - Nov 2022 — **VLSI Design**, *ULP Event Driven Processor*.
Custom designed an ultra low power event driven processor that consumes constant power with temperature and process variations.

Aug - Nov 2019 — **Design for Testability**, *Fault simulation and Fault Coverage Results*.
Implemented Serial fault simulation, parallel fault simulation, parallel pattern fault simulation and deductive fault simulation on various circuits

Jan - April 2020 — **Digital VLSI Design**, *Custom Designing of SRAM and Decoder*.
Simulation and characterization of SRAM, Decoder and SRAM+Decoder Array upto post layout level.

Major Analog Design Projects

Aug- Nov, 2022 — **Monolithic Amplifiers**, *Low Dropout Regulator*.
Designed a fully integrated low dropout regulator based on flipped voltage follower with full spectrum power noise rejection.

Aug- Nov, 2019 — **Adaptive signal procesing**, *A fully integrated analog adaptive disturbance canceller*.
Developed a low power analog adaptive disturbance canceller for high speed circuits.

Aug-Nov,2019 — **ECE Honors**, *A low power time to digital converters for temperature sensors*.
Implemented a time to digital converters for integration with earlier developed temperature to time converter.

Aug-Nov,2018 **Analog IC Design**, *High Speed OTA*.
Designed a high speed OTA with more than 60dB gain and 95V/μs slew rate for high speed applications in UMC 180nm technology. Also worked on slew-boost techniques as part of this course.

Aug-Nov,2018 **ECE Honours**, *Composite Pair Modelling*.
Modelled the composite pair circuit for lower technology nodes by understanding the sub-threshold equations. Later used it to develop voltage reference, current reference and temperature sensor.

Feb-Apr,2018 **Intro to VLSI**, *SAR ADC*.
Designed SAR ADC for bio-medical applications in UMC 180nm tech node.

Feb-Apr,2018 **Intro to VLSI**, *A 10 μW Process Invariant Temperature sensor*.
Designed a composite-pair based process invariant temperature sensor in UMC 180nm technology.

Feb-Apr,2018 **Electronic Workshop 2**, *Composite Light and Sound Synchronization System*.
Designed a synchronized sound and light system using DC-DC converter based LED driver, audio amplifier and analog filters in multisim and implemented it on breadboard.

Jan-Feb,2018 **Electronic Workshop 2**, *Audio Amplifier*.
Designed Audio Amplifier in Multisim and implemented it on breadboard.

Coursework

Monolithic Amplifiers (Prof. Ehsan Afshari), Analog IC Design (RF) (Prof. David Wentzloff), VLSI Design (Prof. David Blaauw), PLL Design (Prof. Micheal Flynn), Analog to Digital Converters (Prof. Micheal Flynn).

Technical Skills

Worked tech-nodes: 180nm, 65nm, 55nm, 28nm, 22nm, 10nm, 7nm, 5nm, 3nm, HVBCD 180nm.

Other Skills: Hspice, C, HTML, Bluespec, Verilog, Matlab, and MIPS.